to connect any of the N columns to any of the M S/H sub-circuits in a first mode of operation, and any other, or combination, of the N columns to any other of the M S/H sub-circuits in a second different mode of operation.

[0062] The processes and devices described above illustrate preferred methods and typical devices of many that could be used and produced. The above description and drawings illustrate embodiments, which achieve the objects, features, and advantages of the present invention. However, it is not intended that the present invention be strictly limited to the above-described and illustrated embodiments. Any modification, though presently unforeseeable, of the present invention that comes within the spirit and scope of the following claims should be considered part of the present invention.

[0063] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An imager device comprising:

a plurality of pixels arranged in at least a first and second column, each column having a column line to which pixels in the column can be connected;

first and second sample and hold circuits for sampling and holding signals output from the pixels on said column lines; and

a multiplexer coupling at least first and second column lines with said first and second sample and hold circuits and being operable, in a first mode, to respectively couple said first and second sample and hold circuits to said first and second column lines and being operable, in a second mode, to respectively couple said first and second sample and hold circuits to said second and first column lines.

2. The imager device of claim 1, wherein the plurality of pixels comprises an array of complementary metal oxide semiconductor pixels.

3. The imager device of claim 1, wherein said multiplexer is controlled such that signals associated with a first pixel type are sampled and held by said first sample and hold circuit and signals of a pixel type different than the first pixel type are sampled and held by said second sample and hold circuit.

4. The imager device of claim 3, wherein the first pixel type is a first pixel color and the pixel type other than the first pixel type is at least a second pixel color.

5. The imager device of claim 3, wherein the first pixel type is a first pixel color and the pixel type other than the first pixel type comprises second and third pixel colors.

6. The imager device of claim 1 further comprising a column decoder connected to and supplying control signals to said sample and hold circuits, said column decoder controlling said sample and hold circuits such that signals associated with a first pixel type are output on a first output channel and signals of a pixel type different than the first pixel type are output on a second output channel.

7. The imager device of claim 6, wherein the first output channel comprises two output lines and the second output channel comprises two output lines.

8. The imager device of claim 7, wherein said first sample and hold circuit samples and holds reset and pixel signals associated with the first pixel type, the pixel signals being output on one output line of the first output channel and the reset signals being output on a second output line of the first output channel.

9. The imager device of claim 7, wherein said second sample and hold circuit samples and holds reset and pixel signals associated with the pixel type that is different than the first pixel type, the pixel signals being output on one output line of the second output channel and the reset signals being output on a second output line of the second output channel.

10. The imager device of claim 1, wherein said multiplexer comprises a plurality of switching circuits.

11. The imager device of claim 10, wherein said switching circuits reside between the pixels and sample and hold circuits.

12. The imager device of claim 10, wherein said switching circuits reside in an input portion of the sample and hold circuits.

13. The imager device of claim 10, wherein said switching circuits comprise one switching configuration when a row being read is an even numbered row and a second switching configuration when a row being read is an odd numbered row.

14. An image device comprising:

a plurality of pixel signals arranged in N columns, each column having a respective column line to which the pixels in the column can be connected;

a plurality Y of sample and hold circuits for sampling and holding signals output from said pixels; and

a multiplexing circuit for coupling, in one operating mode, one of said N column lines to one of said sample and hold circuits and, in another operating mode, coupling a different one of said N columns to said one sample and hold circuit.

15. The imager device of claim 14, wherein each of said M sample and hold circuits comprise respective output lines.

16. The imager device of claim 14, wherein the first operating mode is a readout operation in which even numbered rows of pixels are being read and the another operating mode is a readout operation in which odd numbered rows of pixels are being read.

17. An imager device comprising:

an array of pixels arranged in a plurality of rows and columns, each even numbered row having alternating green and red pixels, each odd numbered row having alternating blue and green pixels;

a plurality of first sample and hold circuits, each first sample and hold circuit being connected to a respective even numbered column of said array;

a plurality of second sample and hold circuits, each second sample and hold circuit being connected to a respective odd numbered column of said array; and

a plurality of switching circuits, each switching circuit being associated with and connected to a respective first sample and hold circuit and its associated even numbered column and a respective second sample and hold circuit and its associated odd numbered column, wherein said switching circuits being controlled such that signals associated with green pixels are sampled and held by said first sample and hold circuits and signals associated with the red and blue pixels are sampled and held by said second sample and hold circuits.

18. The imager device of claim 17, wherein the array of pixels comprises an array of complementary metal oxide semiconductor pixels.

19. The imager device of claim 17, further comprising a column decoder connected to and supplying control signals to said sample and hold circuits, said column decoder controlling said sample and hold circuits such that signals associated with the green pixels are output on a first output channel and signals associated with the red and blue pixels are output on a second output channel.

20. The imager device of claim 19, wherein the first output channel comprises two output lines and the second output channel comprises two output lines.

21. The imager device of claim 20, wherein said first sample and hold circuits sample and hold reset and pixel signals associated with the green pixels, the pixel signals being output on one output line of the first output channel and the reset signals being output on a second output line of the first output channel.

22. The imager device of claim 20, wherein said second sample and hold circuits sample and hold reset and pixel signals associated with the red and blue pixels, the pixel signals being output on one output line of the second output channel and the reset signals being output on a second output line of the second output channel.

23. The imager device of claim 17, wherein said switching circuits reside between the array and sample and hold circuits.

24. The imager device of claim 17, wherein said switching circuits reside in an input portion of the sample and hold circuits.

25. The imager device of claim 17, wherein said switching circuits comprise one switching configuration when a row being read is an even numbered row and a second switching configuration when a row being read is an odd numbered row.

26. The imager device of claim 17, wherein each switching circuit comprises:

a first input switch coupled between a pixel line from the even numbered column and a first charge storage device;

a second input switch coupled between the connection of the first input switch and a third input switch;

said third input switch being coupled between the connection of the third input switch and a fourth input switch; and

said fourth input switch being coupled between a pixel line from the odd numbered column and a second charge storage device.

27. The imager device of claim 26, wherein said first and fourth switches are closed when a row being read is an even numbered row.

28. The imager device of claim 26, wherein said second and third switches are closed when a row being read is an odd numbered row.

29. A processor system comprising:

an imager device comprising:

an array of pixels arranged in a plurality of rows and columns;

a plurality of first sample and hold circuits, each first sample and hold circuit being connected to a respective even numbered column of said array;

a plurality of second sample and hold circuits, each second sample and hold circuit being connected to a respective odd numbered column of said array; and

a multiplexer comprising a plurality of switching circuits, each switching circuit being associated with and connected to a respective first sample and hold circuit and its associated even numbered column and a respective second sample and hold circuit and its associated odd numbered column,

wherein said switching circuits are controlled such that signals associated with a first pixel type are sampled and held by said first

sample and hold circuits and signals of a pixel type different than the first pixel type are sampled and held by said second sample and hold circuits.

30. The system of claim 29, wherein the array of pixels comprises an array of complementary metal oxide semiconductor pixels.

31. The system of claim 29, wherein the pixels of the first pixel type reside in even numbered and odd numbered columns.

32. The system of claim 31, wherein the pixels of the pixel type other than the first pixel type reside in even numbered and odd numbered columns.

33. The system of claim 29, wherein the first pixel type is a first pixel color and the pixel type other than the first pixel type is at least a second pixel color.

34. The system of claim 29, wherein the first pixel type is a first pixel color and the pixel type other than the first pixel type comprises second and third pixel colors.

35. The system of claim 29 further comprising a column decoder connected to and supplying control signals to said sample and hold circuits, said column decoder controlling said sample and hold circuits such that signals associated with the first pixel type are output on a first output channel and signals of a pixel type different than the first pixel type are output on a second output channel.

36. The system of claim 35, wherein the first output channel comprises two output lines and the second output channel comprises two output lines.

37. The system of claim 36, wherein said first sample and hold circuits sample and hold reset and pixel signals associated with the first pixel type, the pixel signals being output on one output line of the first output channel and the reset signals being output on a second output line of the first output channel.

38. The system of claim 36, wherein said second sample and hold circuits sample and hold reset and pixel signals associated with the pixel type that is different than the first pixels type, the pixel signals being output on one output line of the second output channel and the reset signals being output on a second output line of the second output channel.

39. The system of claim 29, wherein said switching circuits reside between the array and sample and hold circuits.

40. The system of claim 29, wherein said switching circuits reside in an input portion of the sample and hold circuits.

41. The system of claim 29, wherein said switching circuits comprise one switching configuration when a row being read is an even numbered row and a second switching configuration when a row being read is an odd numbered row.

42. The system of claim 29, wherein each switching circuit comprises:

a first input switch coupled between a pixel line from the even numbered column and a first charge storage device;

a second input switch coupled between the connection of the first input switch and a third input switch;

said third input switch being coupled between the connection of the third input switch and a fourth input switch; and

said fourth input switch being coupled between a pixel line from the odd numbered column and a second charge storage device.

43. The system of claim 42, wherein said first and fourth switches are closed when a row being read is an even numbered row.

44. The system of claim 42, wherein said second and third switches are closed when a row being read is an odd numbered row.

45. A processor system comprising:

an imager device, comprising:

an array of pixels arranged in a plurality of rows and columns, each even numbered row having alternating green and red pixels, each odd numbered row having alternating blue and green pixels;

a plurality of first sample and hold circuits, each first sample and hold circuit being connected to a respective even numbered column of said array;

a plurality of second sample and hold circuits, each second sample and hold circuit being connected to a respective odd numbered column of said array; and

a plurality of switching circuits, each switching circuit being associated with and connected to a respective first sample and hold circuit and its associated even numbered column and a respective second sample and hold circuit and its associated odd numbered column, wherein said switching circuits being controlled such that signals associated with green pixels are sampled and held by said first sample and hold circuits and signals associated with the red and blue pixels are sampled and held by said second sample and hold circuits.

46. The system of claim 45, wherein the array of pixels comprises an array of complementary metal oxide semiconductor pixels.

47. The system of claim 45, further comprising a column decoder connected to and supplying control signals to said sample and hold circuits, said column decoder controlling said sample and hold circuits such that signals associated with the green pixels are output on a first output channel and signals associated with the red and blue pixels are output on a second output channel.

48. The system of claim 47, wherein the first output channel comprises two output lines and the second output channel comprises two output lines.

49. The system of claim 48, wherein said first sample and hold circuits sample and hold reset and pixel signals associated with the green pixels, the pixel signals being output on one output line of the first output channel and the reset signals being output on a second output line of the first output channel.

50. The system of claim 48, wherein said second sample and hold circuits sample and hold reset and pixel signals associated with the red and blue pixels, the pixel signals being output on one output line of the second output channel and the reset signals being output on a second output line of the second output channel.

51. The system of claim 45, wherein said switching circuits reside between the array and sample and hold circuits.

52. The system of claim 45, wherein said switching circuits reside in an input portion of the sample and hold circuits.

53. The system of claim 45, wherein said switching circuits comprise one switching configuration when a row being read is an even numbered row and a second switching configuration when a row being read is an odd numbered row.

54. The system of claim 45, wherein each switching circuit comprises:

a first input switch coupled between a pixel line from the even numbered column and a first charge storage device;

a second input switch coupled between the connection of the first input switch and a third input switch;

said third input switch being coupled between the connection of the third input switch and a fourth input switch; and

said fourth input switch being coupled between a pixel line from the odd numbered column and a second charge storage device.

55. The system of claim 54, wherein said first and fourth switches are closed when a row being read is an even numbered row.

56. The system of claim 54, wherein said first and fourth switches are closed when a row being read is an even numbered row.

57. A processor system comprising:

an imager device, said imager device comprising:

a plurality of pixel signals arranged in N columns, each column having a respective column line to which the pixels in the column can be connected;

a plurality Y of sample and hold circuits for sampling and holding signals output from said pixels; and

a multiplexing circuit for coupling, in one operating mode, one of said N column lines to one of said sample and hold circuits and, in another operating mode, coupling a different one of said N columns to said one sample and hold circuit.

58. A method of operating an imager device, said method comprising the steps of:

storing signals associated with a first pixel type in a first storage device associated with a first column of pixels;

storing signals associated with a type other than the first pixel type in a second storage device associated with a second column of pixels;

outputting the signals from the first storage device to a first channel; and

outputting the signals from the second storage device to a second channel.

59. The method of claim 58 wherein said step of storing signals associated with the first pixel type comprises:

determining whether a row being read is even; and

if it is determined that the row is even, storing a signal received from a first column in the first storage device.

60. The method of claim 59, wherein said step of storing signals associated with the first pixel type further comprises:

connecting the first storage device to a second column if it is determined that the row is odd; and

storing a signal received from the second column in the first storage device.

61. The method of claim 58, wherein said step of storing signals associated with a pixel type other than the first pixel type comprises:

determining whether a row being read is even; and

if it is determined that the row is even, storing a signal received from a first column in the second storage device.

62. The method of claim 61, wherein said step of storing signals associated with a pixel type other than the first pixel type further comprises:

connecting the second storage device to a second column if it is determined that the row is even; and

storing a signal received from the second column in the second storage device.

63. A method of operating a CMOS color imager device, said method comprising the steps of:

storing signals associated with green pixels in a first storage device associated with a first column of pixels; and

storing signals associated with red and blue pixels in a second storage device associated with a second column of pixels.

64. The method of claim 63 further comprising the steps of:

outputting the signals from the first storage device to a first channel; and

outputting the signals from the second storage device to a second channel.

65. The method of claim 63, wherein said step of storing signals associated with green pixels comprises:

determining whether a row being read is even; and

if it is determined that the row is even, storing a signal received from a first column in the first storage device.

66. The method of claim 65, wherein said step of storing signals associated with the green pixels further comprises:

connecting the first storage device to a second column if it is determined that the row is odd; and

storing a signal received from the second column in the first storage device.

67. The method of claim 63, wherein said step of storing signals associated with the red and blue pixels comprises:

determining whether a row being read is even; and

if it is determined that the row is even, storing a signal received from a first column in the second storage device.

68. The method of claim 67, wherein said step of storing signals associated with the red and blue pixels further comprises:

connecting the second storage device to a second column if it is determined that the row is even; and

storing a signal received from the second column in the second storage device.